"Secure hardware: What are the BIG challenges?"

Session 3: Panel Session
Room 304, Moscone Center, San Francisco
Monday, 27 July, 2009 from 01:15 PM to 2:00 PM
2nd IEEE International Workshop on Hardware-Oriented Security and Trust (HOST)
Co-located event at the Design Automation Conference (DAC)

Format:

Five-minute overview by each panelist, followed by 30-45 minutes of audience participation.

Moderator:

Jim Plusquellic (University of New Mexico)

Panelists:

Miron Abramovici (DAFCA)
CJ Clark (Intellitech Corp.)
Paul Kocher (Cryptography Research)
Ted Huffmire (Naval Postgraduate School)
Ken Mai (Carnegie Mellon University CyLab)
Patrick Schaumont (Virginia Tech)

Presentations:

Detecting Trojans without Golden Models
*Miron Abramovici (DAFCA)*

Tamper Resistance for Field-Programmable Gate Arrays (FPGAs)
*CJ Clark (Intellitech Corp.)*

Security Features for Hardware Design Tools
*Ted Huffmire (Naval Postgraduate School)*

Security: A First-Class Design Constraint?
*Ken Mai (Carnegie Mellon University CyLab)*

Challenges for Secure Hardware
*Patrick Schaumont (Virginia Tech)*